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Comparison and simulation of a highly linear LNA using 45 nm CMOS process

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Abstract:

This paper focuses on the design of low-power and low-noise (LNA) amplifier functions. Various LNA topologies operating with power consumption under milliwatts at a frequency of 2.4 GHz have been implemented in a 40 nm CMOS commercial process . LNA1 (Common Source LNA Cascad) has an efficiency of 12.22 dB، noise coefficient (NF) of 4.35 dB، and third-order input interception point (IIP3) of -12.68 dB at 995.6 µW، while proposed LNA2 has been improved. Linearity has increments of 5.68 dB، 5.13 dB NF، and 0.12-dBm IIP3 Is. The difference between both the final designs, which involve linearity and gain increase, comes from the location of gate inductance () in the Nash chipL_g. The proposed LNA3 with a single chip has an increase in voltage of 11.1 dB, NF 4.27 dB and IIP3 -0.82 dB. In addition, $L_g$the proposed LNA4 with an off-chip chip has an increase in voltage of 10.31 dB, NF 3.68 dB and IIP3 0.89L_g dB at 989.6 µW in post-layout simulations. By comparison LNAs, the proposed LNA4 with an off-chip chip has the best$L_g$merit index (FOM). The goal is to achieve improved linear digits at power below milliwatts.The purpose of this paper is to compare the simulation and comparison between the simulation LNA4 with a 40 nm CMOS technology and a 45 nm CMOS technology. The results of the simulation comparison are included in section 4 of the paper. Although the technology used occupies a slightly larger structure, they still have very close answers.

Keywords: Low power, Improved linearity, Low noise, CMOS, IMD, Linearization, High frequency circuit

1. Introduction

In recent years, wireless technology has become more vital due to the rapid development of health applications, the Internet of Things (IoT) and Bluetooth Low Energy (BLE) applications. For example, using Bluetooth low-energy technology, instant body signals can be monitored through portable and wireless devices. Body temperature and heart rate sensors are also good examples of biomedical applications [1]. These medical devices such as wireless transmitters and implantable antennas should be small and should operate at very low power. Therefore, biomedical wireless transceivers have been significantly improved due to extensive research on transceiver topologies and design of RF circuits using standard CMOS technology.[2]

A low-noise amplifier (LNA) is the first stage of receivers that amplifies filtered radio frequency (RF) signal with as much noise and distortion as possible. A superheterodyne receiver consists of 5 main blocks: an antenna, an RF filter, a low-noise amplifier, a mixer and a voltage-controlled oscillator. The filtered RF signal received from the antenna is mixed with a local oscillator in the RF receiver chain and pre-converted by the LNA Strengthening. After demodulation, the signal is converted down by analog to digital converter, digitized. LNAs, typically the first and one of the most important stages of the receiver, have a large impact on the overall performance of the receiver. In addition, voltage gain and linearity are important performance criteria for LNAs. LNA must have a high voltage for noise suppression of the next steps [4]. However, power consumption limits these performance metrics. Therefore, the main goal is to minimize the balance between power consumption and high performance.Low power performance is a design problem for voltage and noise increases due to low current levels. Also, linearity, which is characterized by the third-order input interception point (IIP3), corresponds to noise factor and voltage gain [5]. Therefore, linear improvement techniques should be applied to develop linear and low-power LNA designs. In this paper, four low-power LNA topologies that are at a frequency of 2.4 GHz Working with submilliwatt power consumption (below 1 mW), they are implemented in a commercial 40-nanometer CMOS technology .

The first scheme, LNA1, has a high voltage gain and low IIP3 digit, while, through linear improvement techniques, the second design, LNA2, offers better IIP3 performance. However, the voltage gain is significantly reduced by the rise of IIP3. The third topology, LNA3, is developed without reducing the performance of IIP3 to increase the voltage gain The difference between the third and last LNA circuit (LNA4) is whether the chipL_g is included or

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not. Hence, this paper focuses on the design challenge of achieving high linearity, even though current levels are very low due to the 1mW power consumption limit. This is a The design problem is difficult because many biomedical tools have to work on limited budgets, but they must deliver high performance. In particular, a highly linear response is expected. This paper shows that, taking LNA4 into account, it is possible to use linear improvement techniques and combine them with design approaches that ensure that voltage gain and noise coefficient are the least effective and remain within their specified range, an IIP3 above 0 dBm produced. In short, the contribution of this work lies in providing design solutions for low-power and high-performance receivers, especially in biomedical applications.

This article has the following structure: The designs of proposed LNAs are described in Part 2. Part 3 discusses the simulation results. Finally, conclusions are drawn in Section 4.

2. Circuit description

The goal of the four LNA schemes in Figure 1 is to operate with power consumption below milliwatts at 2.4 GHz. LNA1 in Figure 1(a) is the classic LNA cascode. LNA2 in Fig. 1(b) is designed to improve the performance M_a of IIP3 by adding as an IMD sine. In LNA3, shown in Figure 1M_b(c), it is added to increase the voltage without reducing the form of IIP3. Also, LNA4 performs the same function as LNA3. It is included L_g as an on-chip component in LNA3 while it remains off-chip in LNA4, such as Figure 1(d). The bias conditions of all LNAs vary slightly, however they all have an overall power consumption of less than 1 mW. Hence, each LNA is optimized for noise coefficient, voltage gain, and linear performance metrics by observing this limit.

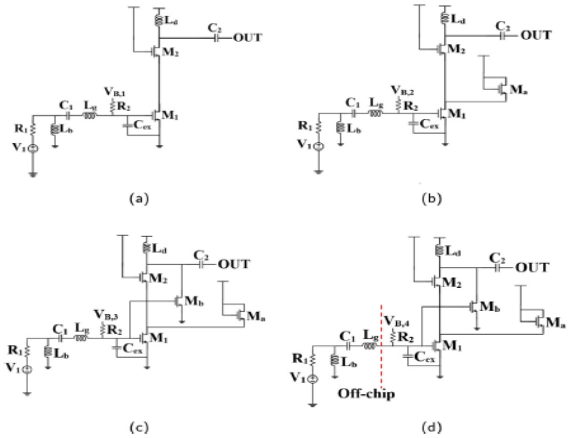

Figure 1-Schematic a) LNA1 b) LNA2 c) LNA3 d) LNA4

Table 1- Executive Characteristics Designed LNAs

S_{11}	< -10 dB
S_{22}	< -10 dB
S_{21}	> 10 dB
NF	< 4 dB
IIP3	> -1 dBm
P_{DC}	< 1 mW
f_C	2.4 GHz

band of Medical Science Industrial (ISM). As can be seen in Table 1, the required

The working frequency of the low-noise amplifier signal should be in the 2.4 GHz

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gain and linearity cannot be freely optimized for this reason.

In Figure 2(a), the transientM_1 is the main istori_2 and the connected diode also states the power as (1)

$$i_2 = i_1 - i_a \quad (1)$$

The$i_1 i_2 i_a$ original source$M_1 M_2 M_a$of IMD3 is derived from third-order nonlinearity, M_1 because the generated nonlinear current is fully transmitted, acting as a flow $M_1 M_2$ buffer. If the discharge hasM_1an additional flow path that selectively cancels the IMD3 flow component, then a flow component The IMD3 is M_2 smaller to be transmitted. Thus, the M_a transistor connected to the diode, which acts as IMD3, is added to the LNA1 as Figure 2(a).

LNA characteristics are determined as an increase in voltage of at least 10 dB and a noise value of less than 4 dB. The input and output reflection coefficients should be less than -10 dB. A low-noise amplifier with less than 1 mW total power Consumes while having IIP3 higher than -1 dB meters. Although the performance specification listed for an LNA with a narrow band is relatively modest, it should be emphasized that the purpose of these criteria is to yield less than 1 mW of power consumption . In this respect, similar to a case of large-band LNA operation, the coefficient cannot be Reduce noise as much as it should because the current required for that performance exceeds the limit imposed by power consumption. Moreover, voltage

The n-MOSFET drain current can be supplied using the power series expansion as follows:

$$i_d = g_{m1} + g_{m2}(V_{gs})^2 + g_{m3}(V_{gs})^3 \quad (2)$$

where theg_{mi} transitionis nth. And also, i_1,in the form of and the poweri_a

$$i_1 = g_{m1,M1} V_{gs1} + g_{m2,M1}(V_{gs1})^2 + g_{m3,M1}(V_{gs1})^3 \quad (3)$$

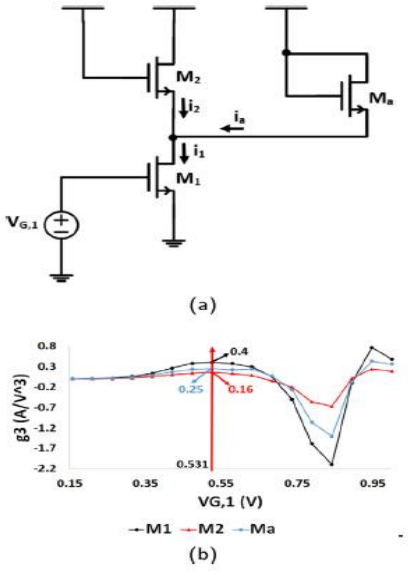

Figure 2- a) LNA With a NMOS Deadly IMD bthe Third Order Transitional Guidance M1,M2,Ma

$$i_a = g_{m1,Ma} V_{gsa} + g_{m2,Ma}(V_{gsa})^2 + g_{m3,Ma}(V_{gsa})^3 \quad (4)$$

ignored. Therefore, the number$i_a$of terms V_{gs1} can be found:

$$i_a = g_{ma,Ma} c_1 V_{gs1} + g_{m2,Ma} c_2 (V_{gs1})^2 + g_{m3,Ma} c_3 (V_{gs1})^3 \quad (6)$$

Considering (2)–(6) to (1), it will be equal to:i_2

Where and so$V_{gs1} V_{gsa}$on stands for gate-source M_1voltage. The function$M_a V_{gsa}$ of the is, thereforeV_{gs1}, can be V_{gsa}extended using the power series,

$$V_{gsa} = c_1 V_{gs1} + c_2 (V_{gs1})^2 + c_3 (V_{gs1})^3 \quad (5)$$

Where c_i the coefficient is dependent on frequency. A first-order approximation is sufficient to prove the cancellation, so the second- and third-order components are

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531 mVHowever, the voltage increase is also due to a decrease in the expression () of the eternal decrease$g_{m1,M1} - c_1 g_{m1,Ma}$. Therefore, as shown in Figure 1(d), add to the voltage gain to increase the voltage gainM_b.

The LNA4 is designed with a high linearity in Figure 1(dL_g), which includes over-the-chip and off-chip versions. The off-chip goal is to obtain L_ga high-quality factor and thus reduce the occupied chip asset.

g_m In LNA without the technique of improving voltage gain is equal to transmitting conductivity, while in $g_{m1,M1} = 11.24\, mS$LNAg_m with the technique of improving the voltage increase, the sum and, $g_{m,M1}$hereby, bringing the total to 13.31 $g_{m,Mb}$mS. IodineM_b measurements are made so that the current balance of IMD is not disrupted to maintain linear operation.

$$i_2 = (g_{m1,M1} - c_1 g_{1,Ma})V_{gs1} + (g_{m2,M1} - c_1^2 g_{m2,Ma})(V_{gs1})^2 + (g_{m3,M1} - c_1^3 g_{3,Ma})(V_{gs1})^3 \quad (7)$$

The coefficients, and depend on the frequency$c_1 c_2 c_3$, and have c_1 a positive sign because 1 draws the current proportionally (M_a Kim and Kim, 2006). In addition, it aims to cancel the byas-gate mode. However, IMD3 is $(g_{m3,M1} - c_1^3 g_{m3,Ma})$ not completely cancelled due to the limited amount of power allocated, so the circuit is designed to minimize the IMD3 component .

In Figure 2(b), the third-order () transconductance diagrams for the $g_{m3}s$, and by taking the derivative of the third order JerianM_1 the $M_2 M_a$ discharge of the corresponding transistor were obtained according to the following. The value ranges from 400 mA/V3 $V_{gs1} g_{m2,M2}$ to 160 mA/V3 and P=986.6µW. $V_{gs1} =$

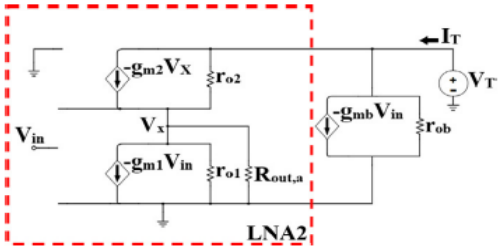

Figure 3- Small signal equivalent Suggested LNAs

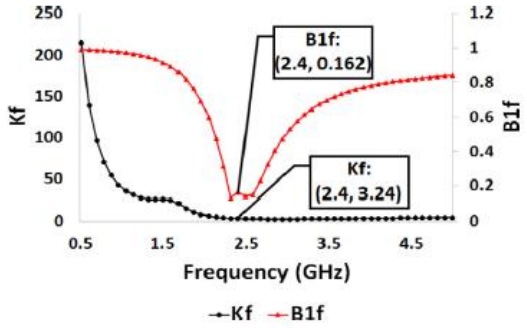

Figure 4- Display values Towards And the doctors. Designed LNAs

LNA1$1/g_{ma} \ll r_{o1}, r_{oa}$. When M_b represented, due to the maximum power requirement of 1 mW, the operating current of the cascaded stage decreases slightly. Reducing cascad stage flow increasesR_{OUT} even if it is inr_{ob} the shunt with cascad exit resistance . Also, AZ, $g_m M_b$ amplifies

The output resistance of LNA2, by adding an eternal dm$R_{OUT} M_a$. In Figure 3$R_{OUT,a}$, it is equal to, while$1/g_{ma})||r_{oa} R_{OUT}$ for LNA1, it is $g_{m2} r_{o2} r_{o1}$ in LNA2$g_{m2} r_{o2} \left(r_{o1} \left|\right| 1/g_{ma} \left|\right| r_{oa}\right)$.

R_{OUT}LNA2 is smaller than

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GHz, respectively. Therefore, itM_b does not reduce LNA stability.

3. Simulation Results and Discussion

The proposed high-linearity LNA is designed in a 40nm commercial CMOS process technology with a supply voltage. $V_{DD} = 1\,V$ Current consumption is 989.6 µA. All LNAs are built and optimized to operate at a frequency of 2.4 GHz. Simulations were performed in Cadence Virtuoso and R+C+CC was selected as the extraction type, which included all the jamming resistances, The jamming capacitors and coupling capacitors are in post-layout simulations. Table 2 presents channel geometry (µm|nm) of transistors and values of components. Channel B length is M_2chosen more than other transistors for larger cascad output resistance. Quality factors are both and L_g 80 L_b which are determined as off-chip inductors. Also the inductor quality factor on the chip L_d is 7.12 evaluated. Figure 5 shows the final layout of the LNA plan, which occupies an area of 0.085 mm2.

LNA, because a Provides voltage gain path in shunt with cascaded amplifier. Increases both and increases$R_{OUT}g_m$ the LNA3 voltage .

A spiral inductor has not been used in the source because the bonded wires previously produced an induction effect there. Typically, band wires have a higher quality factor than spiral inductors, which helps to reduce noise resistance and help with noise. By removing spiral inductors, the total surface area of the chip is also reduced. The inductance value of the bonded wire here is 500 pH It has been selected that may be achieved using two parallel link wires each having a typical inductance of 1 nH.

M_b Directly connected to the input. Hence, stability must be checked. Unconditional stability conditions are shown in terms of S parameters in (8) and (9) [7].

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (8)$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \quad (9)$$

In Figure 4, and K_fB1f, which refer to K and $|\Delta|$, are equal to 3.24 and 0.162 at 2.4

Table ۲- Elements and transistor size ratiosW/L

M_1	32 µm | 40 nm	C_1	200 pF
M_2	16 µm | 150 nm	L_b	750 pH
M_a	8 µm | 40 nm	C_{ex}	712 fF
M_b	44 µm | 40 nm	L_d	8.5 nH
L_g	2.2 nH	C_2	483 fF

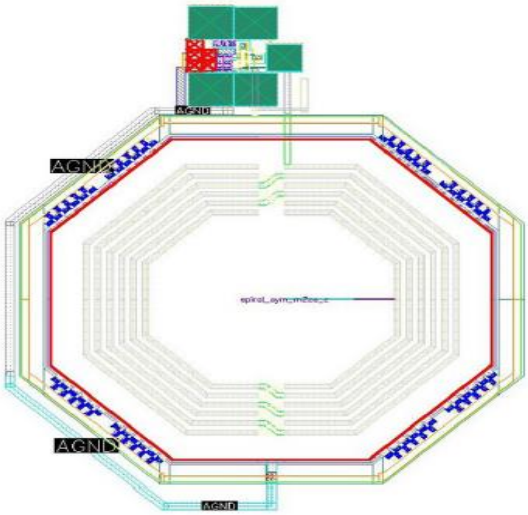

Figure 5- Layout Related to LNA4 Designed

output impedances (respectively db and$S_{11} = -27$des-bell). In Figure 6(a$S_{22} = -17$), it is shown that the

Figure 6(a) and 6(b) shows the performance of LNA1 when set to operate at 2.4 GHz. It has matching input and

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signal. The gate bias and size are set for$M_a$deletion$g_{3,M2}$. Due to the power consumption limit, it cannot be completely removed. However,$g_{3,M2}$ it can be reduced to a sufficient amount of IIP3 to increase the IIP3 value by approximately 12.5 dB/m. In Figure ٨(a) and ٨(b), the performance of LNA٣ is illustrated by linear improvements and voltage gains. This shows that the voltage gain increases by approximately 6 dB without reducing the performance of)IIP٣. Figure ٨a shows that the voltage (gain andNF have improved to 11.1 and 4.27 dB, respectively. In Figure 8 (b), IIP٣ It is ٠٫٨٢-dBm. It is also the values S_{11} and S_{22} less than -١١ dB. Finally, it is stored in the LNAL_g on the chip.

designed LNA1 achieves an increase of 12.22 dB. The noise factor is also 4.35 dB. Finally, Figure 6 ((b) An IIP3 is equal to 12.68 dBm.

Figure 7(a) and 7(b) shows LNA2 performance with improved linearity at 2.4 GHz. Input and output reflection coefficients meet design specifications (dB and dB, respectively). In Figure 7 (a), the voltage gain decreases from 12.2 dB to 5.68 dB, while IIP3 is reduced from 12.68 dB to 0.12 $S_{11} = -17.97 S_{22} = -23$ dB in Figure 7 (b) increased. In addition, NF increased to 5.13 dB.

In Figure 2(b),M_a IIP3 is added to the LNA1. It is alsoM_a used to reduce IMD3 $M_2$with injectable flow. It decreases with the refining$g_{3,M2} g_{3,Ma}$ $g_{3,M1}$ of the same

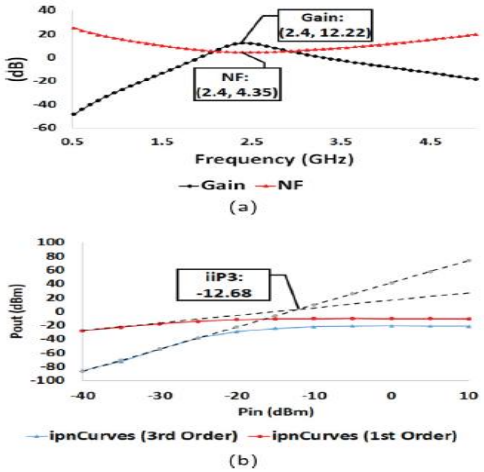

Figure -٦ a Gain Voltage andNF b(IIP3 Related to LNA1

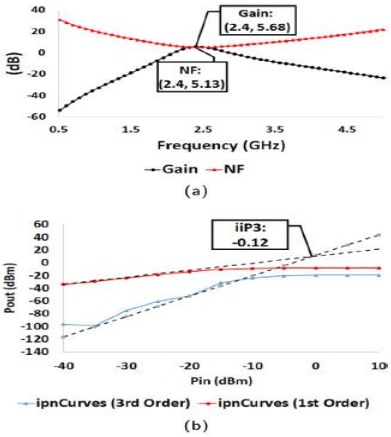

Figure 7- aGain Voltage and NF b) IIP3 Related to LNA2 With improved line

Figure ٣٠ the voltage gain is added to the LNA2 .to increase the voltage gain However، the voltageM_b between the input and output ports of the LNA reduces

While IIP3 decreases by improving $g_{3,M2}$ the indefinitely، the voltage gain through ،the loss in، as shown in (٧)$g_{m,M2}$ decreases theM_b indefinitely. As shown in

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critical in LNA performance in the layout. Therefore, these paths are drawn along with the input and output paths to reduce the wider jamming resistance . Therefore, there is no significant change in and S_{11}It S_{22} is not seen in post-installation simulations.

As seen in Figure 11(a), the LNA designed in post-layout simulations achieves a voltage gain of 10.31 dB. The loss of gain in postlayout simulation results is due to the jamming resistance. Figure 11(b) shows that NF increases with decreasing voltage gain.

,Finally IIP3 was enhanced in post-layout ,simulations compared to pre-layout results as shown in the figures . Figure ١٢(a) and ١٢(b). The induction effect between the source and the ground causes a linear increase and a decrease in gain. The increase in linear results of post-layout simulations arises from source .degeneration due to noise resistances

the cascade which is determined by the parameter.S_{12} is Therefore، IodineM_b measured in such a way that it increases the gain of the voltage without being dominant enough to reduce the separation. This has been investigated in Figure ٩ and it is observed that the ١٣ dB S_{12} has increased but this change in design specifications is , .considered tolerable

Figures 10, 11 and 12 show the functions before and after the LNA layout L_g by improving the linearity and increasing voltage (off the chip). According to Figure 10(a) and 10(b), input and output reflection coefficients at 2.4GHz are acceptable, with$S_{11} = -19.36$ (pre-set) and desibel (after layout) () decibel$S_{11} = -13.35$ (pre-installation) and$S_{22} = -21.21$desibel $S_{22} = -15.42$(after layout). The S_{22} is important because the designed LNA is modular. Hence, it can be applied to different receiver structures. DC lines that pass through the incoming RF path are

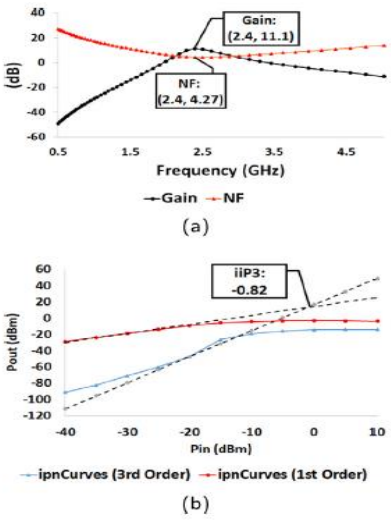

Figure -٨ a Gain Voltage andNF b (IIP3 Related to LNA3With linear and improved voltage gain

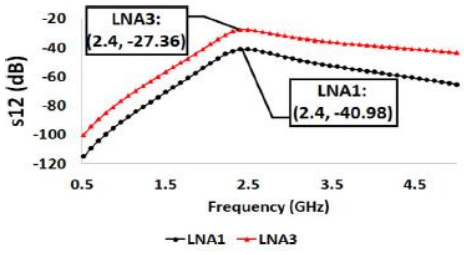

Figure 9- S12 Related to LNA1 and LNA3

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table 3-Run LNA4 In different processes and temperatures

Temperature	SS			FF			FS			SF		
	0 °C	25 °C	75 °C	0 °C	25 °C	75 °C	0 °C	25 °C	75 °C	0 °C	25 °C	75 °C
S_{11} (dB)	−9	−9	−9	−8.75	−9.33	−10.6	−12	−13.0	−14.6	−12.7	−13.6	−15.4
S_{22} (dB)	−22.6	−21.1	−19	−13.4	−12.9	−12.3	−15.6	−15.0	−14	−16.9	−16.5	−15.8
S_{21} (dB)	7	6.57	5.65	13.5	13.22	12.7	11	10.64	9.88	10.4	9.99	9.2
NF (dB)	4.5	4.99	5.97	2.36	2.64	3.2	3.22	3.6	4.35	3.33	3.72	4.5
IIP3 (dBm)	7.73	8.18	7	−2.56	−2.69	−2.43	−0.20	−0.32	−0.07	4.38	3.69	3.74

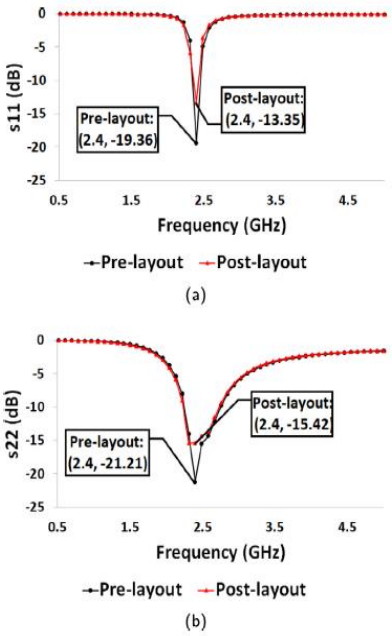

Figure -١٠ a (S11 b(S22 Related to LNA4With improved line and voltage gain

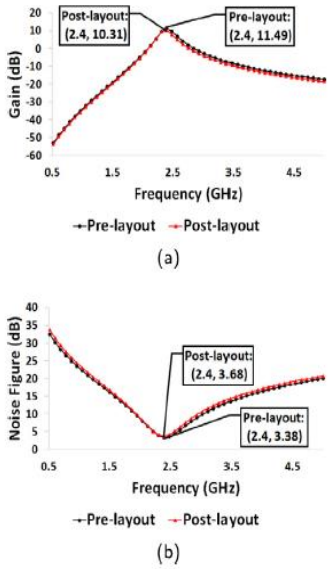

Figure 11- aGain Voltage b) NF Related to LNA4 With improved line and voltage gain

temperature decreases, the voltage rise increases whileNF decreases. Degraded SS forS_{11} and FF process corners. Other than that, other performance parameters .are acceptable

The performance parametersof LNA4 are simulated in four different process corners (SS ,FF, FS, and SF) andthree different temperatures (0◦C, 25◦C and 75◦C). The results are presented in Table 3. As the

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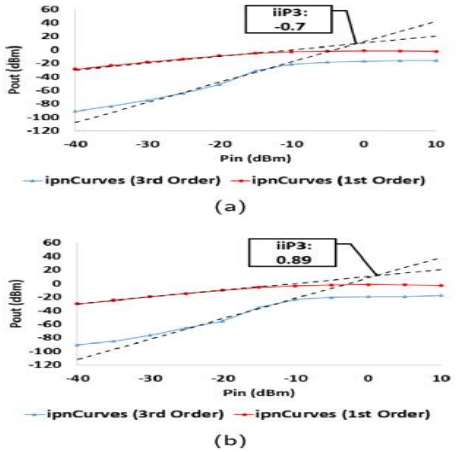


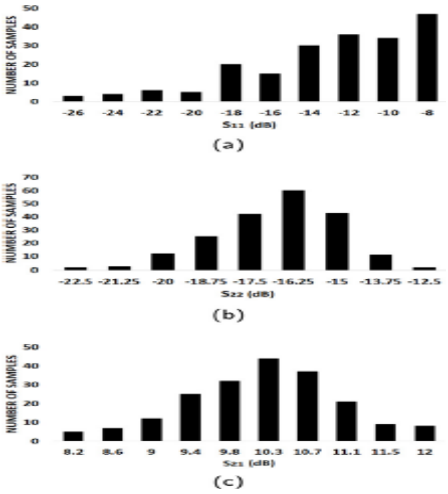
Figure -١٢ IIP3 a (Pre-Layoutb (Post-LayoutLNA4With linear and improved voltage gain

table 4-Analysis MC Related to LNA4

	Best value	Worst value	Mean
S_{11} (dB)	−27.2	−8.53	−14.01
S_{22} (dB)	−24.52	−12.09	−16.91
S_{21} (dB)	12.19	7.99	10.24
NF (dB)	2.95	4.66	3.73
IIP3 (dBm)	9.44	−5.27	2.2

table ٥-RunSuggested LNAs

	LNA1	LNA2	LNA3	LNA4 (pre-layout)	LNA4 (post-layout)
S_{21} (dB)	12.22	5.68	11.1	11.49	10.31
NF (dB)	4.35	5.13	4.27	3.38	3.68
S_{11} (dB)	−27	−17.97	−21	−19.36	−13.35
S_{22} (dB)	−16	−23	−14.78	−21.21	−15.42
IIP3 (dBm)	−12.68	−0.12	−0.82	−0.7	0.89
P1dB (dBm)	−23.74	−12.13	−13.57	−11.54	−11.16
P_{DC} (μW)	995.6	986.6	997.2	1079	989.6
FOM	0.198	1.36	2.82	6.10	7.05



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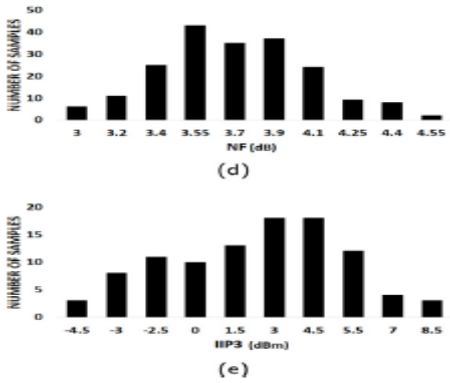

Figure 13Differences in the histogram parameters in Monte Carlo simulation. a) S11 b) S22 C) S21 D) NF e) IIP3

IIP3) in Figure 13. Table 4 lists the worst, best, and average values of performance parameters obtained in the MC simulation.

The performance of LNA4 is also examined under process changes and mismatches using Monte Carlo analysis (MC) of more than 200 samples (100 for

table 6- Compare the proposal with others LNAha

	Gain (dB)	NF (dB)	IIP3 (dBm)	P_{dc} (μW)	F_c (GHz)	Tech. (nm)	FOM
This Work (post-layout)	10.31	3.68	0.89	989.6	2.4	40	7.05
[12] (measurement)	11	6.8	−2.2	174	2.4	65	6.56
[13] (post-layout)	18.2	3.38	−4.32	967	2.4	180	2.93
[14] (post-layout)	14	3.45	−8	980	2.4	180	0.92
[8] (pre-layout)	14	5.2	−8.6	30	2.4	40	15.2
[15] (measurement)	12.6	5.5 ~6.5	−9	750	0.1~7	90	0.47
[16] (measurement)	12.3	4.9~16	−9.5	400	0.1~2.2	130	0.87
[17] (measurement)	14	4~6	−10	250	0.6~4.2	130	1.87
[18] (measurement)	17.4	2.8	−10.7	480	2.4	65	1.71
[9] (measurement)	13.9	8.9	−13	69	2.4	65	1.27
[19] (measurement)	12.2	1.9~2.2	−16	350	3~5	130	0.97
[10] (measurement)	21.5	6.3	−16	900	2.4	28	0.11
[11] (measurement)	6.9	3	−18	44	2.4	16	1.25
[20] (post-layout)	13.64~15.64	4.5~6	−5~ -6	600	0.03~3	180	1.30
[21] (measurement)	16.8	6.6	−16.4	350	4	28	0.20

In Table 6, the performance criteria of LNA4 are compared with the different results of low-power LNAs reported in the paper with working frequency in the range of 0.1 GHz to 7 GHz. Although the FOM [8] is higher than that of LNA4, its IIP3 is roughly equal to LNA1 . Except [8], LNA4 in terms of value FOM is the best among all comparable studies. In addition, power consumption [9] is substantially low. However, its NF is very high, and the amount of IIP3 reported is much lower than the LNA4 design described in this work. Also, [10] and [11] are notable in terms of the use of CMOS technologies at the deep nanoscale. However, NF [10] is very high, while voltage gainers [11] are significantly low.

4. Comparison of simulation

The results of theory and simulation have been achieved by ۴۰nm $S_{21} = 12 - 19$ dB .process but in the process of ۴۵ nm dB Similarly, other parameters are decibel and dB, but in other processes for M_3 $S_{21} = 11.287 S_{11} = -27.2 S_{22} = -24.52 S_{11} = -9.646 S_{22} = -9.961$ dB and also noise coefficient is ۲/۹۵ dB in ۴۰ nm process and

Table 5 summarizes the performance of four different LNAs. While LNA1 is not suitable for satisfying linear specifications, the performance of IIP3 has improved dramatically by approximately 12.5 mB in LNA2, thus meeting the requirements. However, the voltage gain and NF LNA2 are much lower than the specifications. Although the voltage gain and performance of IIP3 in LNA3 Enhanced, this topology may occupy a large chip area due to the input matching circuit on the chip. By removing the outside of the chip, all L_gLNA4 performance subordinates conform to the basic design specifications. Since it is $L_g$off-chip, it can be considered a high quality factor that further improves overall performance. When the number of competencies (FOM) calculated based on the expression presented in (10), compared out of the four LNA topologies, LNA4 is the most successful of all in terms of performance metrics achieved.

$$\text{FOM} = \frac{\text{Gain (dB)} \times \text{IIP3 (μW)}}{(\text{NF (dB)} - 1) \times \text{Power (μW)}} \quad (10)$$

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and ۱۴, and the summary of the ۱۵ ,۱۴ .results is also shown in the table

in ۴۵ nm process equal to4.9 dB is obtained. The results are shown in Figures

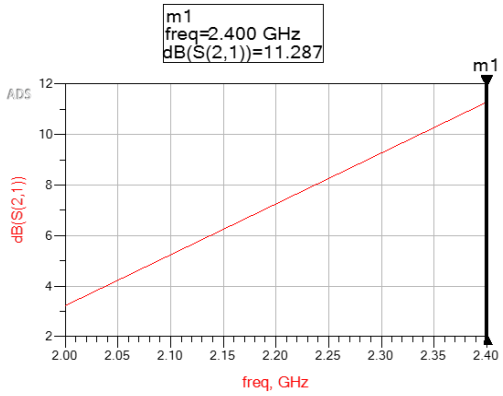

Figure -۱۴ S21 Related to LNA4۴۵nm

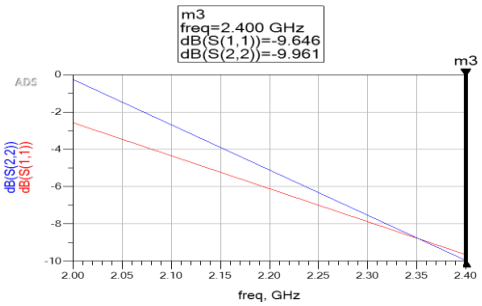

Figure 15- S11 and S22 Related to LNA4 45nm

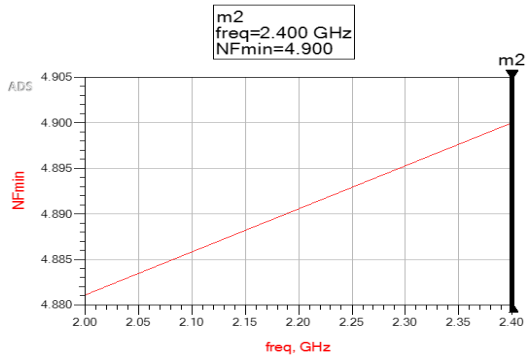

Figure 16- NF Related to LNA4 45nm

.table ۷A summary of the results of the simulation

V_{DD}	I_{DD}	Power	Technology	S_{21}	BW	Noise
1v	815uA	815uW	Cmos 45nm	11.2dB	2400MHz	4.9dB

5. Conclusion

In this paper, four LNAs are designed using two different techniques to improve linearity and gain voltage in power below mW in a 40-nm CMOS commercial process at 2.4 GHz. The proposed LNA, LNA4, with a 1 volt power supply, achieves an IIP3 digit of 0.89 dBm and wastes 989.6 microwatts at 2.4 GHz. It has a voltage gain of 10.31 dB and a noise coefficient of 3.68 dB. Based on its design criteria, LNA4 can be used in very low-power and high-performance receivers, as it is often encountered in biomedical applications.

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